In the claims:

Please substitute the following full listing of claims including new claims 17 and 18 for the claims as originally filed or most recently amended.

1. - 12. (Canceled)

13. (Previously Presented) A heterojunction bipolar transistor, comprising:

a collector region;

a SiGe base region;

an emitter stack overlaying said collector region, said emitter stack including an emitter opening filled with T-shaped polysilicon, said T-shaped polysilicon overlaying nitride regions included in said stack, and said emitter stack including an implant-masking cap layer on top of said T-shaped polysilicon, and wherein said emitter stack does not have spacers; and

one and another extrinsic base regions arranged on respective sides of said emitter stack, said extrinsic base regions being directly aligned with said emitter polysilicon region but not being directly aligned with said emitter opening.

14. (original) The transistor of claim 13, wherein said extrinsic base regions are made from SiGe polysilicon.

15. (Previously Presented) The transistor of claim 13, wherein said one of said extrinsic base regions is longer than said another of said extrinsic base regions, and wherein a base contact is formed on the longer extrinsic base region.

16. (currently amended) The transistor of claim 13, wherein said collector region, emitter stack, and extrinsic base regions are contacted using mid-end-of-line collector, emitter, and base contacts respectively.

17. (New) The transistor as recited in claim 13, wherein said emitter stack comprises less than five layers.

18. (New) The transistor as recited in claim 13, wherein said emitter stack comprises only an oxide layer, a nitride layer and a TEOS layer.

19. (New) The transistor as recited in claim 13, wherein said T-shaped polysilicon layer in said pedestal has substantially equal lengths on both sides providing substantially equal base resistance, whereby base resistance of said transistor may be minimized.